Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method for modeling a semiconductor device process, comprising:

(a) setting data of an SiO_2 layer;

(b) setting data of an Si layer brought in contact with said SiO_2 layer;

(c) setting a plurality of cells in said Si layer, and setting an amount of an impurity included in each of said cells;

(d) setting an amount per unit time by which said impurity included in each of said cells moves to another cell;

(e) setting data by which a cell in a vicinity of an interface of said SiO_2 layer and said Si layer is set as an impurity pileup portion;

(f) setting data of a position of a source or a drain in said Si layer; and

(g) calculating the amount of said impurity included in each of said cells for each unit time after processing said steps (a) through (f),

wherein ~~a mass~~ an amount of said impurity in each of said cells moving to said impurity pileup portion from each of said cells is determined as an impurity density as a

function of a distance r1 to said impurity pileup portion from each of said cells, and a function of a distance r2 to said source or said drain from each of said cells.

Claim 2 (Original): The method for modeling the semiconductor device process according to claim 1 wherein the data of the position of said source or said drain is set so that said source or said drain is distributed in a predetermined region in said Si layer, and said distance r2 is a distance between each of said cells and said predetermined region.

Claim 3 (Currently Amended): The method for modeling the semiconductor device process according to claim 1 wherein the movement [[mass]] amount of said impurity is determined as a function of a solid angle considering each of said cells set as said impurity pileup portion from each of said cells.

Claim 4 (Original): The method for modeling the semiconductor device process according to claim 1, further comprising setting data in which a part of said impurity is generated or disappears for each unit time.

Claim 5 (Currently Amended): The method for modeling the semiconductor device process according to claim 1, wherein said ~~step(f)~~ step (f) comprises:

assuming that a plurality of said sources or said drains exist in said Si layer; and

setting data in which the data of a position of a specified one of said sources or a data of a position of a specified one of said drains is able to be ignored selectively.

Claim 6 (Currently Amended): The method for modeling the semiconductor device process according to claim 1, further comprising:

(h) storing data representing a magnitude of a reverse short channel effect; and

(i) calculating a threshold voltage using the impurity amount calculated during said ~~stop(g)~~ step (g).

Claim 7 (Currently Amended): The method for modeling the semiconductor device process according to claim 1, further comprising setting data of ~~an other~~ another insulating layer disposed on a side of said Si layer opposite to said SiO_2 layer ~~via said Si layer~~.

Claim 8 (Currently Amended): The method for modeling the semiconductor device process according to claim 1, wherein the function of the distance r1 is

$$\exp(-r1/\lambda 1),$$

wherein the function of the distance r2 is

$$\exp(-r2/\lambda 2), \text{ and}$$

wherein $\lambda 1$, $\lambda 2$ are source and drain process dependent parameters, wherein $\lambda 1 = 2.0\mu m$ and $\lambda 2 = 0.5\mu m$.

Claim 9 (Currently Amended): The method for modeling the semiconductor device process according to claim 1, wherein the [[mass]] amount of said impurity moving to said pileup portion from each of said cells is determined as a product of the function of the distance r1 and the function of the distance r2.